

Rapid thermal annealing of *in situ* p-doped polycrystalline silicon thin-films

W. AHMED, A. AFZAL

Department of Chemistry and Materials, Faculty of Science and Engineering,
Manchester Metropolitan University, Chester Street, Manchester, M1 5GD, UK
E-mail: w.ahmed@mmu.ac.uk

Polycrystalline silicon thin films deposited via low-pressure chemical vapour deposition (LPCVD) have a rough surface and a resistance which is too high for use within microelectronic devices. However, both of these problems may be overcome by *in situ* doping of the polycrystalline silicon films with phosphorus by introducing PH_3/N_2 and SiH_4/N_2 mixtures simultaneously into a LPCVD reactor but, such doping requires a high temperature furnace step ($\cong 950^\circ\text{C}$) to bring the resistivity down to the required level. In general, prolonged exposure to high temperature is undesirable since it not only reduces the resistivity of the polycrystalline silicon film but also disturbs the existing dopant profiles and alters the structure of the films deposited. This ultimately makes the devices fabricated unreliable, difficult to reproduce and thus a broad device specification in batch production. The solution is to decrease the furnace temperature or reduce the time the devices are kept at high temperature. The latter may be achieved by using a technique known as rapid thermal annealing (RTA). In this paper we examine rapid thermal annealing as a quick method of redistributing the dopants in order to achieve a lower sheet resistance. The results obtained are compared with conventional furnace annealing. It will be shown that rapid thermal annealing is an attractive and often better alternative to conventional annealing. © 1999 Kluwer Academic Publishers

1. Introduction

Low-pressure chemical vapour deposition (LPCVD) has become a well established technology for the deposition of polycrystalline silicon, silicon nitride, silicon oxide and semi-insulating polysilicon thin films for the manufacture of microelectronic devices [1–3]. Normally, for the deposition of polysilicon, 100% silane is introduced into the LPCVD reactor at $\cong 630^\circ\text{C}$ resulting in the deposition of thin films of silicon which have a polycrystalline structure. The structure of the deposited films is highly dependent upon the reactor temperature since below 580°C amorphous films are formed whereas polycrystalline films are formed above this temperature [4]. However, both the resistivity and the surface roughness of the resulting polycrystalline silicon films are too high for many microelectronic devices. High temperatures of the order of 950°C in an atmosphere of nitrogen are used to anneal the polysilicon films and a lower resistance is achieved by introducing small amounts of phosphorus, boron or arsenic into the films. Phosphorus doping may be achieved by introducing POCl_3 at a high temperature or alternatively by introducing 1% PH_3 in N_2 during LPCVD simultaneously with 100% silane in order to reduce the film resistance. *In situ* phosphorus doping is potentially very attractive since deposition and doping can be carried out in a single step thus reducing both processing time and cost. However, it results in poor uniformity and low growth

rates [5–7]. The within-wafer uniformity degrades from better than $\pm 3\%$ for undoped films to worse than $\pm 60\%$ in many cases for doped films. Growth-rates drop dramatically from about $100 \text{ \AA}/\text{min}$ for undoped films to less than $10 \text{ \AA}/\text{min}$ for *in situ* phosphorus-doped films. These problems have been investigated extensively. Low deposition rates have been overcome by using a more reactive precursor of silicon e.g. disilane which increases the deposition rate of *in situ* doped polysilicon by over 20 orders of magnitude. For undoped polycrystalline silicon the deposition rate from disilane is nearly twice that achieved when silane was used as a silicon precursor [8]. Poor within-wafer uniformity has been considerably improved using either wafer cages or ultra-low pressures [9, 10]. Regardless of the silicon precursor used the problems of high resistivity and rough surface still persist. Although the arguments presented in this work relate to *in situ* doping using silane, they are highly likely to be equally valid for deposition based on disilane. In this paper we compare conventional and rapid thermal annealing of *in situ* phosphorus doped silicon. The electrical characteristics of the polycrystalline silicon films subjected to these two methods of annealing and dopant activation are compared. A reduction in processing time and control are obvious advantages of rapid thermal annealing over conventional annealing.

2. Experimental

The LPCVD reactor employed in this study is commonly used in the semiconductor industry and has been described previously [4]. The reactor consists of a diffusion furnace and a fused silica tube. A fused silica boat is normally used to hold wafers in a close-packed vertical arrangement in an axially symmetrical position in the tube. The reactor is pumped by a two-stage rotary pump. A Baratron gauge is used to measure the reactor pressure, with typical pressures in the range of 0.1–1 torr. Mass flow controllers with a range of 0–100 sccm are normally employed. A motorised throttle valve or nitrogen mass flow controller are commonly used to control the reactor pressure.

Annealing was done either in a conventional furnace at 800–950 °C in a nitrogen atmosphere for 30 to 50 min or using a rapid thermal annealer 2101 model AG Associates at $\cong 1200$ °C for 30–90 s. The sheet resistance, spreading resistance and grain size were measured.

3. Results and discussion

The sheet resistance as a function of annealing time for *in situ* doped polycrystalline films annealed at 950 °C for 30 min in an atmosphere of nitrogen is shown in Fig. 1. Unannealed *in situ* phosphorus doped films gave a value of 190 Ω/\square for 2000 Å thick coatings. This dropped rapidly to about 70 Ω/\square after annealing for 30 min. A further 20 min anneal of the same sample caused a decrease in resistivity to 50 Ω/\square . A resistivity value of 42 Ω/\square was achieved after another 10 min anneal. Hence, initially the resistivity drops rapidly for the first 30 min which may be attributed largely to the activation and redistribution of dopant moving from the grain boundaries into the crystallites. The dopant atoms in the crystallites are active and reduce the resistance of the films whereas those in the grain boundaries are trapped and inactive. Further anneals reduced the resistivity as a result of grain growth which increases active phosphorus present in the crystallites and decreases defect levels. Grain growth increases the relative volume of the crystallites to grain boundaries which in turn reduces the resistance of the films.

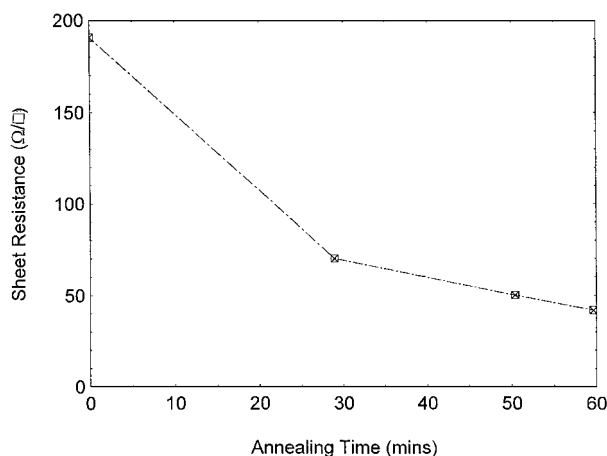


Figure 1 Sheet resistance as a function of annealing time for *in situ* doped polycrystalline films using conventional annealing.

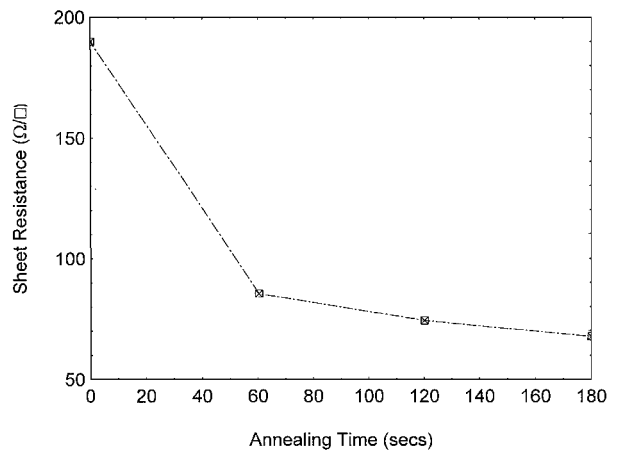


Figure 2 The effect of annealing time on the sheet resistance for *in situ* doped silicon deposited at 630 °C in an inert nitrogen atmosphere using rapid thermal annealing.

It was found that longer periods of time at high temperatures caused a redistribution of dopants in existing device structures therefore it is attractive to employ methods capable of activating dopants much more quickly. This may be achieved via rapid thermal annealing (RTA) where high temperatures are employed for very short periods between 30 to 60 times less than conventional annealing. Fig. 2 shows the effect of annealing time on the sheet resistance for *in situ* doped silicon deposited at 630 °C in an inert nitrogen atmosphere. After 60 s the sheet resistance drops dramatically due to dopant activation to a value of about 80 Ω/\square . A second anneal for 60 s resulted in a drop in the resistivity to a value of 75 Ω/\square . However, subsequent anneals showed very little changes in sheet resistance. It was concluded that no further reduction in sheet resistance took place because 60 s annealing time was not sufficient to initiate and sustain grain growth. Most of the dopants present had been activated i.e., moved from the grain boundaries into the crystallites.

An important consideration, in addition to sheet resistance, is the distribution of dopants within the film as a function of depth. The dopant distribution and spreading resistance for various depths are shown in Fig. 3. From the same figure it is evident that the sheet resistance is not uniformly distributed but, there is a variance in the unannealed sample of the *in situ* doped

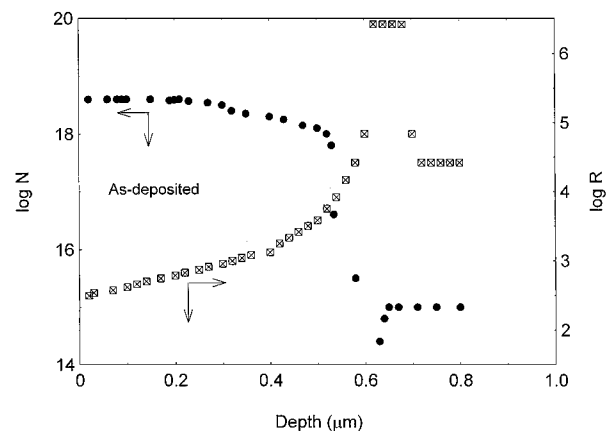


Figure 3 The dopant distribution and spreading resistance as a function of depth.

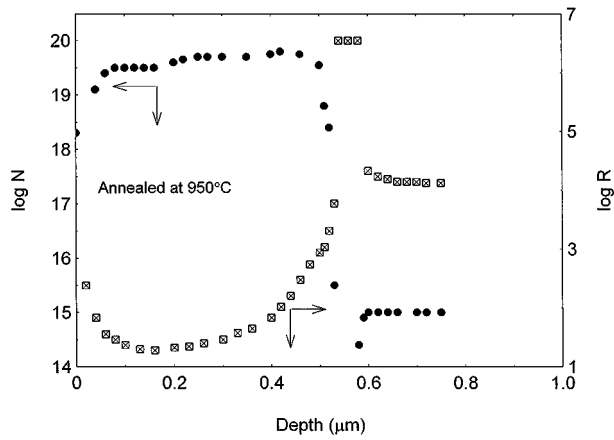


Figure 4 Dopant levels and spreading resistance as a function of depth for *in situ* doped films annealed at 950 °C for 30 min in a nitrogen atmosphere using conventional annealing.

polysilicon films. Spreading resistance only measures dopants that are active and excludes inactive dopants trapped within the grain boundaries. The total dopant level is the sum of the active and inactive dopants (i.e., the sum of dopants in the crystallites and dopants in the grain boundaries). As already mentioned it is believed that annealing redistributes dopants within the film resulting in a more uniform profile. This is clearly evident from Fig. 4 which shows the dopant levels and spreading resistance of *in situ* doped films annealed at 950 °C for 30 min in a nitrogen atmosphere. In this film the phosphorus is more uniformly distributed. Interestingly, the dopant level at the surface as well as the average value is somewhat higher than the unannealed sample. This supports our hypothesis that dopants may move out of grain boundaries and into the crystallites thus becoming electrically active. Simultaneously, grain growth during annealing reduces the defect levels available to trap the dopants once again contributing to a high amount of active dopants. Further investigation using a technique that can measure total dopant content such as secondary ion mass spectrometry (SIMS) would be useful for both annealed and unannealed samples to further validate the above hypothesis.

Fig. 5 shows the variation in carrier concentration and spreading resistance with film thickness for *in situ*

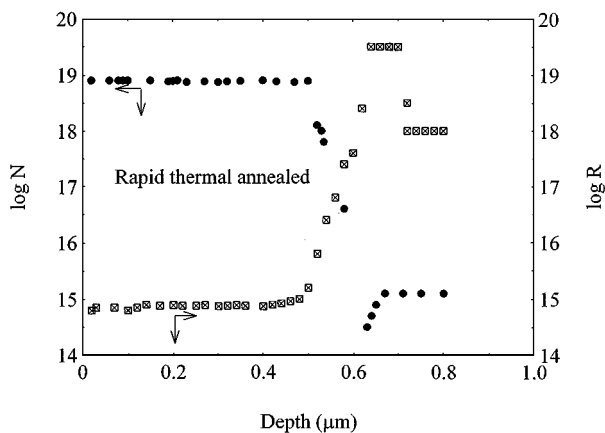


Figure 5 The variation in carrier concentration and spreading resistance with film thickness for *in situ* doped polycrystalline silicon samples annealed in nitrogen for 30 s at 1200 °C using rapid thermal annealing.

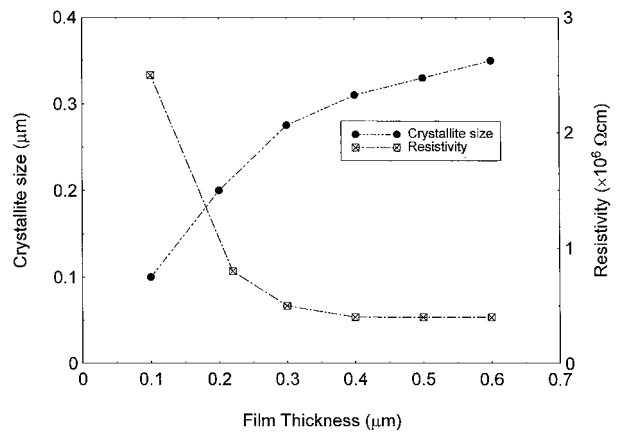


Figure 6 Crystallite size and film resistivity as a function of film thickness.

doped polycrystalline silicon samples annealed in nitrogen for 30 s at 1200 °C via RTA. The rapid thermal annealing method gives a much more uniform dopant profile which is similar to that obtained for conventional annealing. As previously, the dopant concentration is also higher. This can be explained by the movement of the phosphorus out of the grain boundaries and into the crystallites which also corresponds to a decrease in spreading resistance.

Finally, measurements of crystallite size were carried out at different film thicknesses for *in-situ* doped films which had been annealed using RTA for 60 s and the results obtained are shown in Fig. 6. These results show that as the film thickness increased, the crystallite size also increased. For film thicknesses of 0.1 μm, the average crystallite size is about 0.1 μm on average which increases to about 0.26 μm for film thicknesses of about 0.3 μm. The average crystallite size eventually reaches to about 0.35 μm for films that are 0.6 μm thick. The crystallite size increases rapidly for the lower film thickness range but increases gradually for thicker films. As expected from our previous arguments relating to active and inactive dopants in the crystallites and grain boundaries respectively, the film resistivity follows the opposite trend to the grain size. The film resistivity drops rapidly for thinner films and then levels off for thicker films. Examination of crystallite shapes show them to have 'V' shaped appearance when examined using cross-sectional TEM. As the film gets thicker the average grain size is thus expected to increase rapidly and then level off. Near the interface there are many more grain boundaries than crystallites and thus more inactive phosphorus present compared to active phosphorus. This results in a high film resistivity for thinner films compared to thicker films. As the film thickness increases, less grain boundaries relative to crystallites are present which corresponds to a reduction in resistivity.

4. Conclusions

In situ phosphorus doped polycrystalline silicon films have been annealed using both conventional and RTA. Results from resistivity, dopant concentration, spreading resistance and crystallite size measurements are presented and compared. It has been shown that RTA gives

uniform dopant profiles, is highly effective for activating inactive phosphorus, requires much less processing time and is therefore an attractive alternative to conventional annealing for *in situ* phosphorus doped films.

References

1. S. M. SZE, "VLSI Technology," (McGraw Hill Book Company, Singapore, 1983).
2. R. S. ROSLER, *Solid State Technology* **20**(4) (1977) 63.
3. M. L. HITCHMAN and K. F. JENSEN, "Chemical Vapour Deposition: Principles and Applications," (Academic Press, London, 1993) chap. 1.
4. W. AHMED, R. D. PILKINGTON and D. B. MEAKIN, *Thin Solid Films* **202** (1991) 97.
5. B. S. MEYERSON and W. OLBRICHT, *J. Electrochem. Soc.* **131** (1984) 2361.
6. B. S. MEYERSON and M. L. YU, *ibid.* **131** (1984) 2366.
7. K. F. JENSEN, M. L. HITCHMAN and W. AHMED, Proceedings of the Fifteenth International Conference on CVD, Upsala, Sweden, 1985, edited by J. D. Carlson and J. Lindstrass, published by University of Upsala, Sweden.
8. M. L. HITCHMAN, W. AHMED, S. SHAMLIAN and M. TRAINOR, *Chemtronics* **2** (1993) 99.
9. H. KURAKAWA, *J. Electrochem. Soc.* **129** (1982) 2620.
10. W. AHMED, E. AHMED and M. L. HITCHMAN, *J. Mater. Sci.* **30** (1995) 4115.

*Received 18 November 1998
and accepted 7 April 1999*